**BIRLA INSTITUTE OF SCIENCE AND TECHNOLOGY PILANI, HYDERABAD CAMPUS**

**DIGITAL DESIGN LABORATORY (Session 2021-22)**

**Workbook**

**Experiment -9**

**Full Name of the Student: Shyam N V**

**Complete ID of the student: 2020A7PS2081H**

**Title of Experiment: Experiment 9**

**Problem 1:**

**Design an Odd parity generator using Decoder where use the Decoder as a Verilog module.**

**(Provide proper snapshots and Show the graphical output)**

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**Problem 2:**

**Design an Odd parity generator using Multiplexer where use the MUX as a Verilog module.**

**(Provide proper snapshots and show the graphical output)**

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